New Approach to the Design of Active Floating Inductors in MMIC Technology

Salim Georges El Khoury

Abstract— **An original method for the determination of all possible inductive circuits as a function of the number of field-effect transistors (FET's) used is described in this paper. The method is of general use in monolithic microwave integrated circuits. Circuits with large inductance, either positive or negative in value, can be obtained along with low loss or even negative resistance.**

I. Introduction

THE utilization in monolithic microwave/millimeter-wave integrated circuit (MMIC) technology of a spiral inductor in the design of oscillators and filters leads to multiple problems.

1) Dependence of the inductance value on its physical size.
2) Difficulties in reaching inductance values greater than 6 nH.
3) The impossibility of reducing the associated series resistance to zero.
4) Continual presence of significant parasitic capacitances which lead to a reduction in self-resonant frequency thus limiting the useful operating frequency range of the resulting active inductor.
5) The most promising solution to realizing integrated filters seems to be with active inductors. Since 1988, the tentative circuits proposed in [1]–[5] are particular topologies of active inductances with minute losses. These two-port circuits contain a limited number of field-effect transistors (FET's) (2, 3, or 4) which can be represented by the RLC parallel circuit as indicated in (Fig. 1).

The chief advantage of the active-inductor circuits published to date is the appearance of a greater value of inductance ($L_m = 20\,\text{nH}$) but the loss caused by the resistor ($R_m = 500\,\Omega$) is not negligible. Also, the presence of a nonnegligible capacitance of about C_{gs} ($C_m = 0.05\,\text{pF}$) limits the foreseen advantage.

The circuits that have been found so far were mostly obtained by trial and error. To this day, there has not been a systematic study of all of the possible active-inductor circuits topologies.

This paper describe a general method to build inductive circuits and categorizes the topologies according to the number of FET's used. Groups of active floating inductors are described where some groups have a high Q value and others have a negative resistance. The C_m capacitance is reduced (0.01 pF) in both cases.

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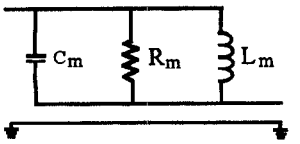


Fig. 1. Equivalent circuit of the active floating inductor.

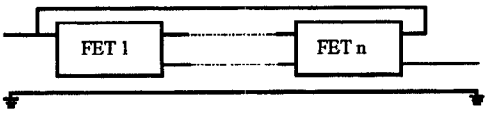


Fig. 2. Adopted form for the inductive circuits.

II. Design Approach

The adopted form will be a cascading chain of FET's with a feedback loop toward the inlet (Fig. 2). Due to the increasing number of all possible combinations, we divide the six possible connections of a FET according to the Y matrix of their simple model (the transconductance gm and the gate-source capacitance C_{gs}) into three classes.

A. Inductor Containing Two FET's

The position of each FET in the circuit (Fig. 3) determines its classification as either class 1, class 2, or class 3. Since there are two FET's and three classes, the possible number of combinations is $3^2 = 9$ and the symmetry of class 1 with comparison to class 2 reduces the number of distinct combinations to six. Each combination possesses ($2^2 = 4$) different circuits. We calculate the Y matrix of each combination (Fig. 4). Among these six combinations, three of them possess a symmetrical and nonvoid Y admittance. As a result, the number of circuits giving rise to floating inductors is equal to $3 \times 4 = 12$. The study shows that four out of 12 circuits [Fig. 5(a) and Fig. 6(a)] indicate a Y admittance equivalent to that of a parallel RLC circuit. These circuits having a positive [Fig. 5(b)] or negative inductance [Fig. 6(b)], where suffixes one and two correspond to the first and second FET, respectively.

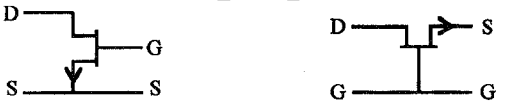
These four circuits will be called elementary cells.

B. Inductor Containing Three FET's

The configuration is shown in Fig. 7. The number of possible combinations is $3^3 = 27$ of which 15 combinations

Class 1

$$Y=\begin{bmatrix}0 & A\\ 0 & B\end{bmatrix}$$



$$Y=\begin{bmatrix}0 & g_m\\ 0 & p\,C_{gs}\end{bmatrix} \qquad Y=\begin{bmatrix}0 & -g_m\\ 0 & g_m+p\,C_{gs}\end{bmatrix}$$

Class 2

$$Y=\begin{bmatrix}A & 0\\ B & 0\end{bmatrix}$$

$$Y=\begin{bmatrix}p\,C_{gs} & 0\\ g_m & 0\end{bmatrix} \qquad Y=\begin{bmatrix}g_m+p\,C_{gs} & 0\\ -g_m & 0\end{bmatrix}$$

Class 3

$$Y=\begin{bmatrix}A & -A\\ -B & B\end{bmatrix}$$

$$Y=\begin{bmatrix}g_m+p\,C_{gs} & -g_m-p\,C_{gs}\\ -p\,C_{gs} & p\,C_{gs}\end{bmatrix} \qquad Y=\begin{bmatrix}p\,C_{gs} & -p\,C_{gs}\\ -g_m-p\,C_{gs} & g_m+p\,C_{gs}\end{bmatrix}$$

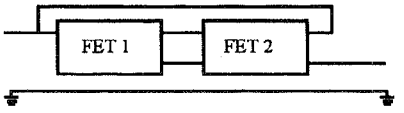


Fig. 3. Configuration of the inductor containing two FET's.

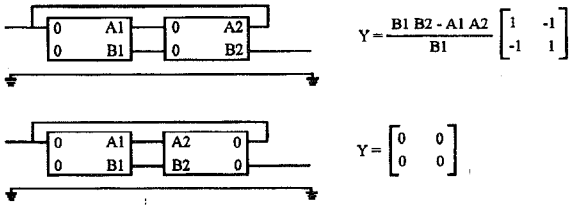


Fig. 4. The Y matrix of the different connections with two FET's.

are different. Each combination possesses $(2^3 = 8)$ distinct circuits. If we calculate the Y admittance matrix of each combination (Fig. 8) we find seven in which the Y admittance matrix is symmetric and nonvoid and therefore $(7 \times 8 = 56)$ different circuits. Those circuits give rise to an active floating inductor.

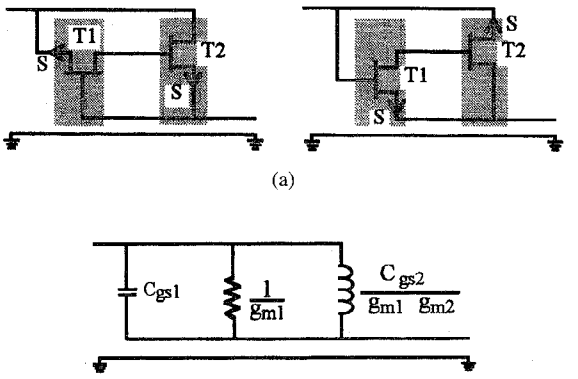


Fig. 5. Elementary cells of the floating positive active inductor. (a) Circuit configuration. (b) Equivalent circuit.

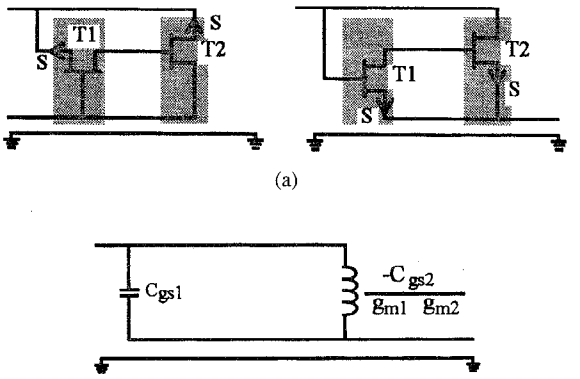


Fig. 6. Elementary cells of the floating negative active inductor. (a) Circuit configuration. (b) Equivalent circuit.

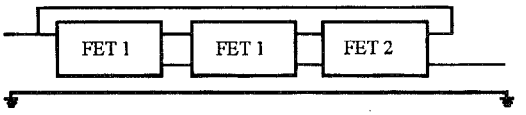


Fig. 7. Configuration of the inductor containing three FET's.

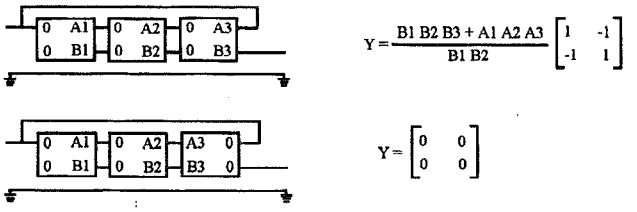


Fig. 8. Matrix Y for different connections with three FET's.

The study of these 56 circuits shows six positive inductors (Fig. 9) and six negative inductive circuits (Fig. 10). Their equivalent RLC circuit creating, in general, a larger inductor with a higher resistor. Only three of these twelve circuits have already been published.

C. Rule of Design

A close examination of the inductive circuits, two FET's in Figs. 5 and 6 and three FET's in Figs. 9 and 10, allows us

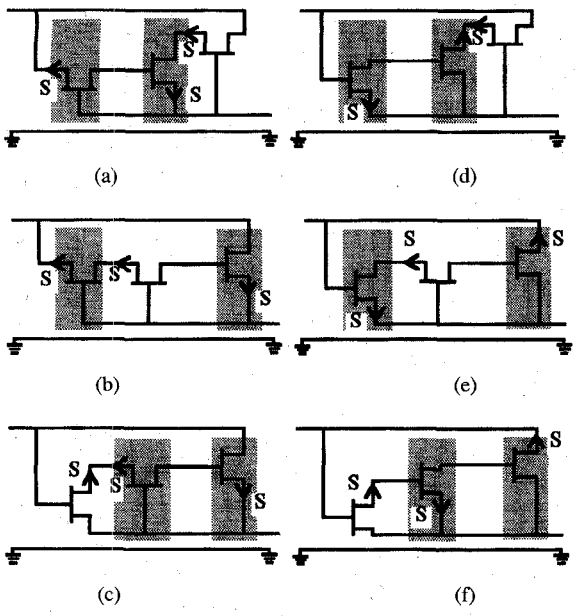


Fig. 9. Circuit configurations of the floating active positive inductor with three FET's. (a) IEEE 1989. (b) Electronics letters, 1991. (c) New. (d) New. (e) IEEE 1993. (f) New.

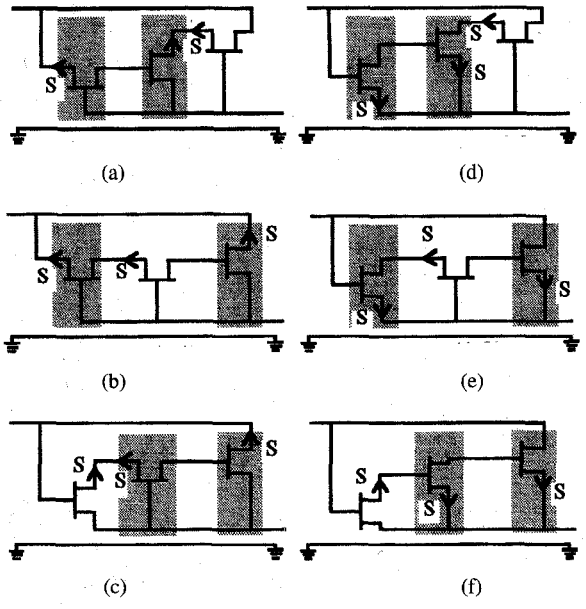


Fig. 10. Circuit configurations of the floating active negative inductor with three FET's. (a) New. (b) New. (c) New. (d) New. (e) New. (f) New.

to discover the rule governing the evolution of the inductive circuits from the elementary cells. In fact, it is the addition of a FET in the beginning, middle, and end of the elementary cell following the schematic shown in Fig. 11 which gives the inductive circuits three FET's.

A four-FET inductor can be conceived by adding a combination of two among these three forms of the FET on the elementary cells following the schematic in Fig. 12. A five-FET inductor can be conceived by adding a combination of three and so on.

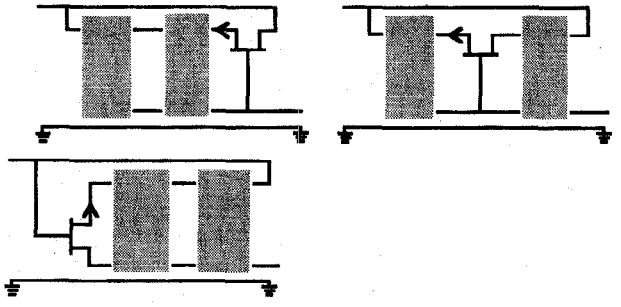


Fig. 11. Evolution of the inductive circuits from the elementary cells.

D. Verification of the Rule in the Case of Four FET's

The inductive circuits generated from the first positive elementary cell are as follows in Fig. 13. We verify by simulation on Libra software that the 24 circuits generated from the four elementary cells are inductive circuits. We also notice that the four FET's inductive circuits possess a larger inductor. This inductor is in parallel with a larger or negative resistor.

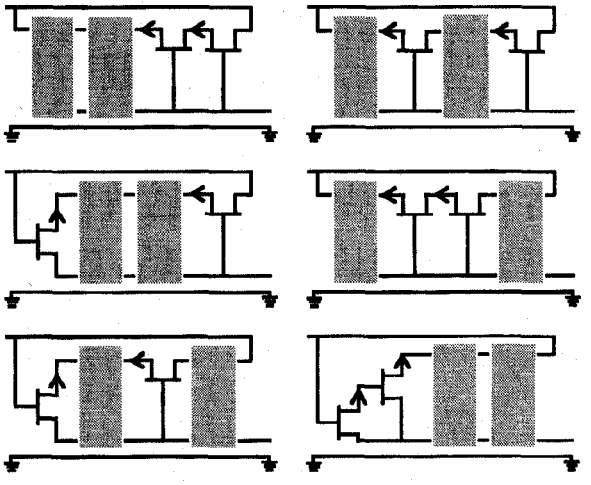


Fig. 12. Determination of the all inductive circuits with four FET's.

III. Other Family of Active Inductors with Large Losses

The study of the two FET circuits also shows the existence of two positive inductors. Their inductance (L_m) is weaker and the losses are more important when compared to the losses in the elementary cells.

The inductive circuits (with n FET's) generated from those circuits (Fig. 14) according to the same designing rule also represent a weaker inductance than that of the inductive circuits generated from the elementary positive cells (Figs. 9 and 13), as well as the most important losses.

The similitude between the circuit shown in Fig. 14(e) and the circuit shown in Fig. 9(c) make Fig. 14(e) the best circuit among those of Fig. 14 and Fig. 9(c), the lesser among those shown in Fig. 9.

The study of circuit at two FET's also shows the existence of two negative inductive circuits, having smaller inductance, and more important losses than those of the negative elementary cells. The circuits generated from these possess the same properties.

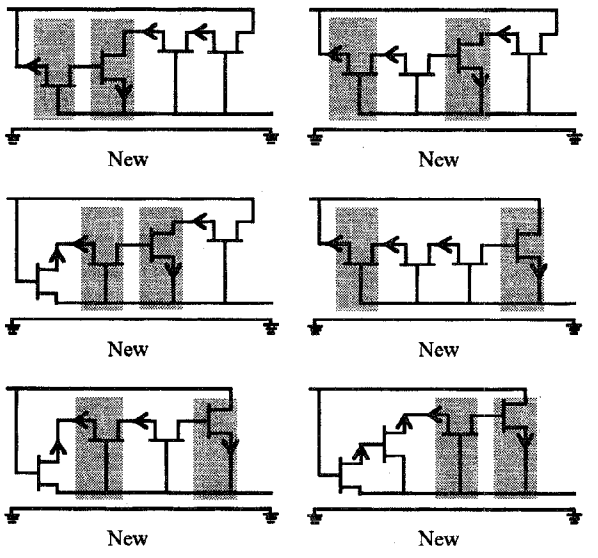


Fig. 13. Circuit configurations of the floating active inductor, with four FET's, generated from the first elementary cell.

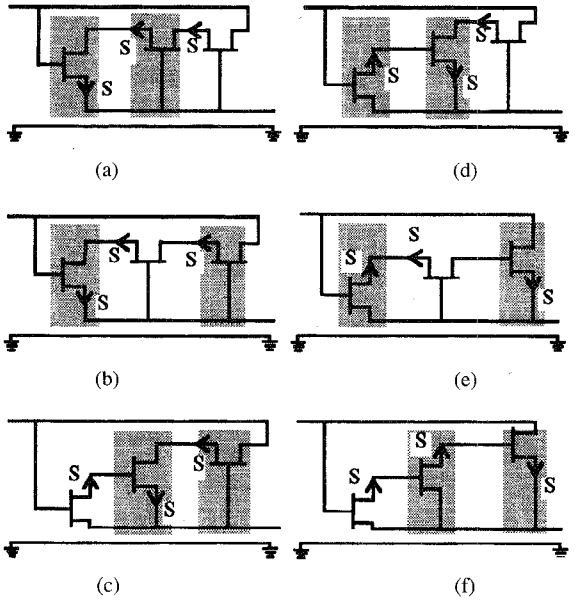


Fig. 14. Inductive positive circuits having large losses.

Thus inductors with large losses can be obtained if a FET in common drain is added at the end of each elementary cell, or another elementary cell.

IV. Quality Factor Improvement

To improve the quality factor of all inductive circuits found by the method described above, we insert a resistor R in the feedback loop. This insertion increases the value of the inductor (L_m) as well as the resistor (R_m) and significantly decreases the value of the parallel capacitance (C_m). Putting it differently, the cut-off frequency increases, and this widens the range of utilization.

In the following, we will consider in more detail the influence of an added resistor first on the elementary cells and then on the three FET inductors.

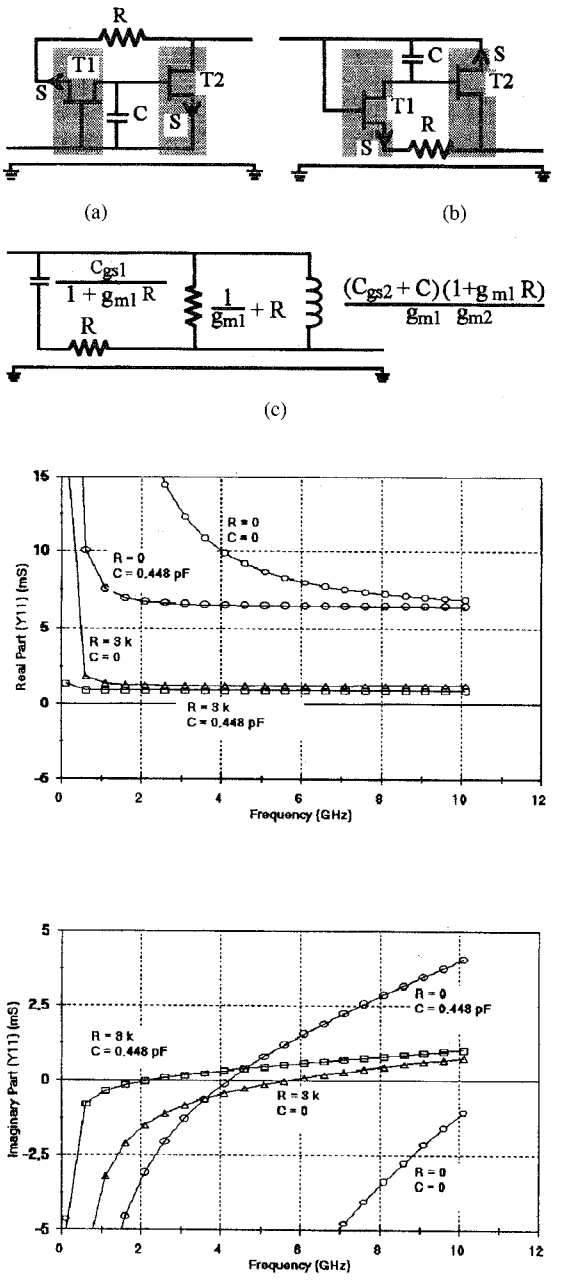


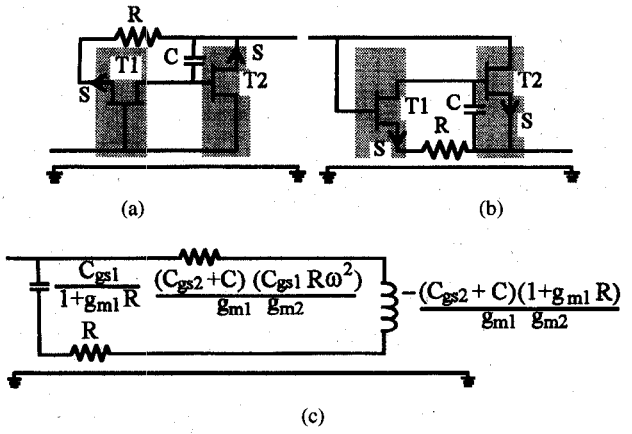
Fig. 15. First influence of the resistor (R) and the capacitance (C) on the elementary positive cells. (a) and (b) Circuit configuration. (c) Equivalent circuit.

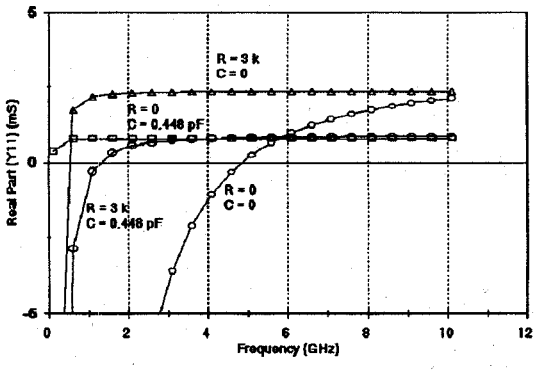
A. Two FET Inductor

Fig. 15(a) and (b) and Fig. 16(a) and (b) display the considered inductors. In the framework of a simple model for the FET (the transconductance gm and the gate-source capacitance C_{gs}) the admittance of Fig. 15(a) and (b) is given by

$$Y = \frac{p(C_{gs2}+C)(g_{m1}+pC_{gs1})+g_{m1}g_{m2}}{p(C_{g2}+C)(1+R(g_{m1}+pC_{gs1}))}\begin{vmatrix} 1 & -1 \\ -1 & 1 \end{vmatrix}.$$

The equivalent circuit is drawn on Fig. 15(c). In this representation, we neglected the effect of the other components on the global behavior of the circuit for frequencies lower than 2 GHz. Note that the increase on the second FET capacitance





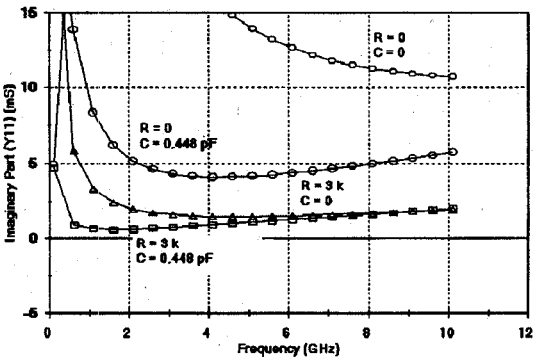


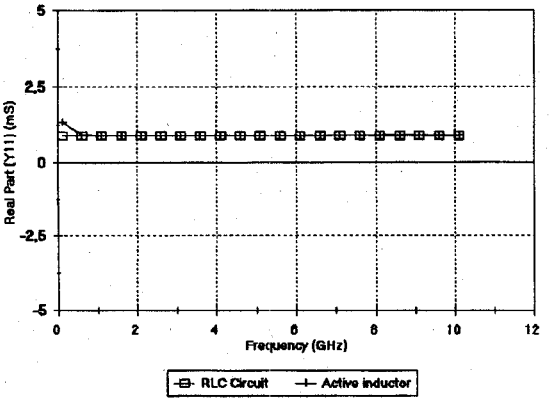
Fig. 16. Influence of the resistor (R) and the capacitance (C) on the elementary negative cells. (a) and (b) Circuit configuration. (c) Equivalent circuit.

(C_{gs2}), by adding a parallel capacitor (C), increases the inductance (L_m).

With a complete model for the FET: $g_m = 5.36\,\text{mS}, C_{gs} = 0.0522\,\text{PF}, C_{gd} = 8\,\text{fF}, C_{ds} = 8.9\,\text{fF}, g_d = 0.5\,\text{mS}$ (when 40 mm gate-width FET's are used), at 2 GHz, for different values of (R) and (C) we find (Fig. 15)

$R\,(\Omega)$	$C\,(\text{pF})$	$L_m\,(\text{nH})$	$C_m\,(\text{pF})$	$R_m\,(\Omega)$	$Q\,(\text{at}\,2\,\text{GHz})$
0	0	3	0.07	50	1.3
0	0.448	18	0.075	155	0.6
3k	0	44	0.17	833	1.5
3k	0.448	300	0.17	1100	0.3

with a simple model for the FET (the transconductance gm and the gate-source capacitance C_{gs}); the admittance of the



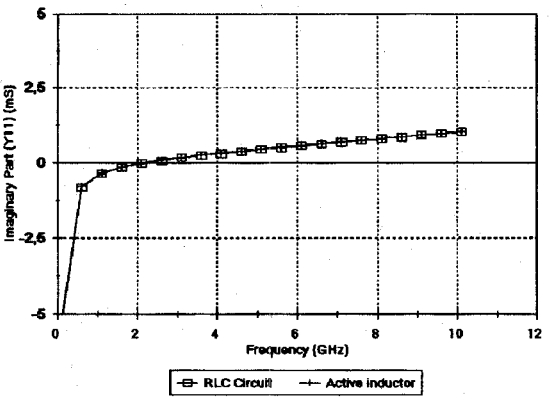


Fig. 17. Comparison of the admittance of the active inductive circuit [Fig. 15(a)] with that of the ideal inductive circuit RLC where $L = 300\,\text{nH}, R = 1.1\,\text{k}\Omega, C = 0.017\,\text{pF}$.

circuit shown in Fig. 16 (a) and (b) is given by

$$Y = \frac{-g_{m1}g_{m2} + p^2 C_{gs1}(C_{gs2}+C)}{p(C_{gs2}+C)(1+R(g_{m1}+pC_{gs1}))} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}.$$

The equivalent circuit is shown in Fig. 16(c). Note that the increase on the second FET capacitance (C_{gs2}), by adding a parallel capacitor (C), increases the inductance (L_m).

With a complete model for the FET: $g_m = 5.36\,\text{mS}, C_{gs} = 0.0522\,\text{PF}, C_{gd} = 8\,\text{fF}, C_{ds} = 8.9\,\text{fF}, g_d = 0.5\,\text{mS}$ (when 40 mm gate-width FET's are used)

for $R = 0, C = 0.448$ pF, we found (Fig. 16):

$$L_m = -20\,\text{nH}, R_m = 1200\,\text{W}, C_m = 0.075\,\text{pF}$$

for $R = 3\,\text{kW}$, $C = 0.448$ pF, we find (Fig. 16):

$$L_m = -300\,\text{nH}, R_m = 1300\,\text{W}, C_m = 0.03\,\text{pF}.$$

Curves on Figs. 17 and 18 show a comparison of the real and imaginary parts of the admittance for circuits Figs. 15(a) and 16(a), respectively, with that of the ideal RLC, when $(R) = 3\,\text{k}\Omega$ and $(C) = 0.445\,\text{pF}$. This curves prove than the representation of the inductive circuit by a parallel RLC circuit is appropriate.

N.B. Our study shows that adding a resistor on the elementary cells, according to (Fig. 19) improves their functioning, but loss efficiently. In effect, we find for $R = 3\,\text{k}\Omega$ and $C = 0.448\,\text{pF}$

$$L_m = 25\,\text{nH}, \quad R_m = 500\,\Omega, \quad C_m = 0.032\,\text{pF}.$$

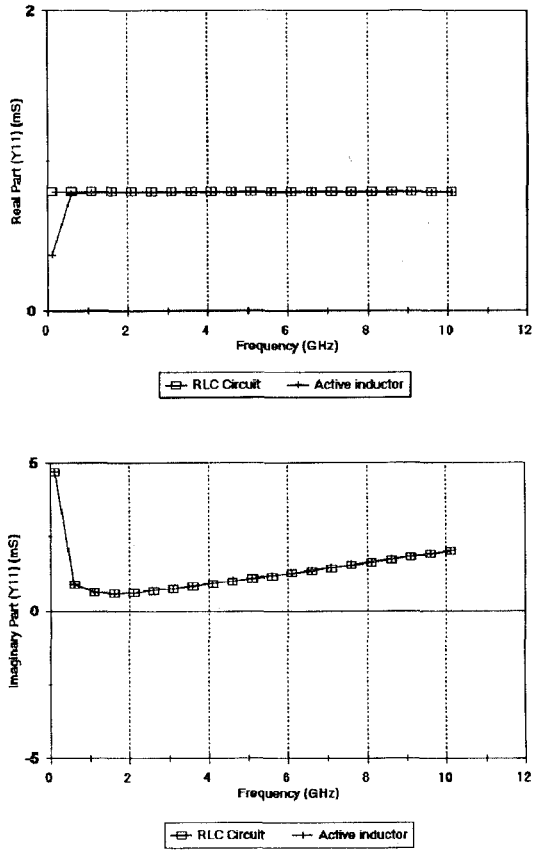


Fig. 18. Comparison of the admittance of the active inductive circuit [Fig. 16(a)] with that of the ideal inductive circuit RLC where $L = -300\,\text{nH}$, $R = 1.3\,\Omega$ and $C = 0.03\,\text{pF}$.

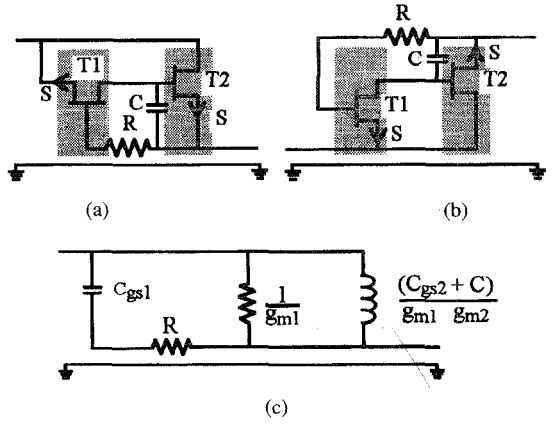


Fig. 19. Second influence of the resistor (R) on the elementary positive cells. (a) and (b) Circuit configuration. (c) Equivalent circuit.

Adding two resistors according to Figs. 15 and 19, simultaneously, on every elementary cell cumulates the improvements for both cases.

B. Three FET Positive Inductors

To increase the quality factor of these inductors, according to the previously described method, we add a resistor in the feedback loop of the circuits generated from the first elementary cell. For the positive circuits generated from the second elementary cell we add a resistor between its second FET drain and the preceding FET as shown in Fig. 20. For those generated from the second negative elementary cell, the resistor is added between its second FET source and the preceding FET (Fig. 21).

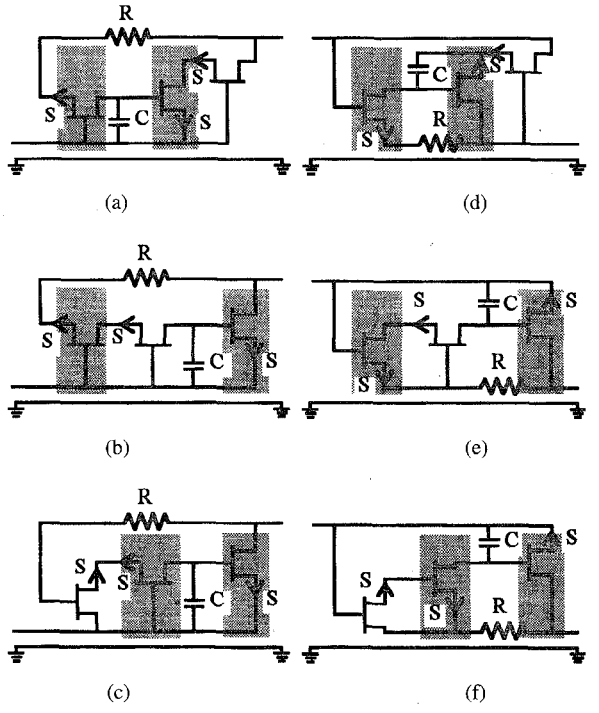


Fig. 20. Circuit configurations of the improved floating active positive inductor with three FET's.

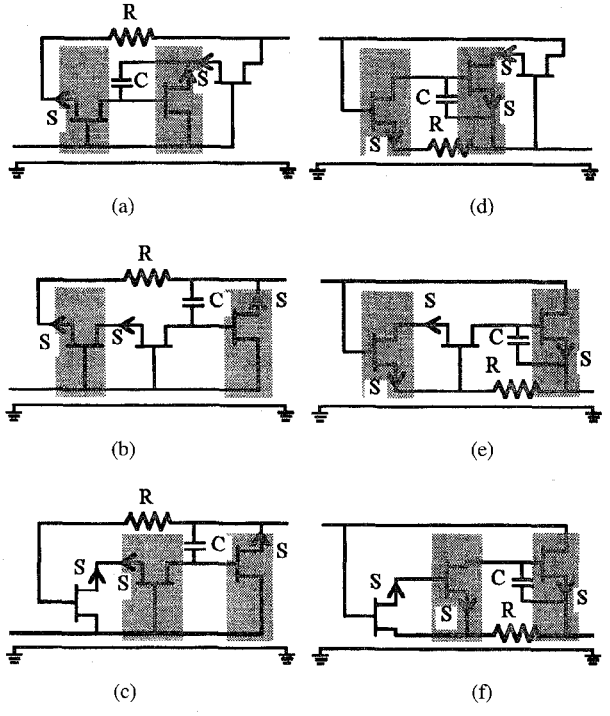


Fig. 21. Circuit configurations of the improved floating active negative inductor with three FET's.

TABLE I
INFLUENCE OF THE RESISTOR (R) AND THE CAPACITANCE (C) ON THE L_m, G_m, C_m FOR EQUIVALENT CIRCUIT OF THE ACTIVE POSITIVE INDUCTOR

	R (Ω)	C(pF)	Lm(nH)	Cm(pF)	Gm(mS)	1/Q
Fig 20a	0	0	3.5	0.08	12.6	0.554
	0	0.448	20	0.08	5.60	1.407
	3k	0	52	0.017	0.07	0.045
	3k	0.448	340	0.016	0.31	1.324
Fig 20b	0	0	3	0.08	3.80	0.143
	0	0.448	18	0.085	5.47	1.237
	3k	0	44	0.017	0.97	0.536
	3k	0.448	320	0.017	0.87	3.498
Fig 20c	0	0	5	0.055	4.9	0.307
	0	0.448	36	0.055	0.68	0.307
	3k	0	10	0.02	-5.4	-0.678
	3k	0.448	38	0.02	0.71	0.321
Fig 20d	0	0	4	0.075	11.2	0.563
	0	0.448	25	0.06	4.25	1.335
	3k	0	63	0.025	-0.55	-0.435
	3k	0.448	340	0.02	0.128	0.546
Fig 20e	0	0	3	0.09	2.71	0.102
	0	0.448	19	0.07	4.85	1.158
	3k	0	38	0.018	1.07	0.511
	3k	0.448	300	0.018	0.88	3.317
Fig 20f	0	0	3	0.06	13.1	0.494
	0	0.448	20	0.05	5.52	1.387
	3k	0	38	0.017	1.42	0.678
	3k	0.448	300	0.017	0.92	3.468

TABLE II
INFLUENCE OF THE RESISTOR (R) AND THE CAPACITANCE (C) ON THE L_m, G_m, C_m FOR EQUIVALENT CIRCUIT OF THE ACTIVE NEGATIVE INDUCTOR

	R (Ω)	C(pF)	Lm(nH)	Cm(pF)	Gm(mS)	1/Q
Fig 21a	0	0	-3.5	0.08	-8.05	0.354
	0	0.448	-20	0.08	0.794	-0.199
	3k	0	-60	0.16	0.0533	-0.401
	3k	0.448	-350	0.16	0.174	-0.765
Fig 21b	0	0	-2.5	0.075	5.95	-0.187
	0	0.448	-18	0.1	1.54	-0.348
	3k	0	-43	0.023	2.648	-1.430
	3k	0.448	-300	0.032	0.849	-3.2
Fig 21c	0	0	-6	0.06	-3.08	0.232
	0	0.448	-42	0.062	-1.646	0.868
	3k	0	-15	0.02	7.762	-1.463
	3k	0.448	-40	0.03	1.151	-0.578
Fig 21d	0	0	-3.5	0.06	-5.542	0.243
	0	0.448	-21	0.07	0.491	-0.129
	3k	0	-55	0.023	1.217	-0.841
	3k	0.448	-375	0.028	0.223	-1.050
Fig 21e	0	0	-3.5	0.06	0.886	-0.038
	0	0.448	-20	0.075	1.288	-0.323
	3k	0	-38	0.027	1.867	-0.891
	3k	0.448	-320	0.03	0.673	-2.706
Fig 21f	0	0	-4	0.05	-5.141	0.258
	0	0.448	-22	0.05	0.884	-0.244
	3k	0	-40	0.03	1.546	-0.777
	3k	0.448	-350	0.03	0.635	-2.792

Our study shows that the increase of the gate-source capacitance of the second FET of the elementary cell increases the inductance (Lm) whatever the position of the FET in the circuit. This increase of the capacitance will be realized by adding a parallel capacitor (see Figs. 20 and 21).

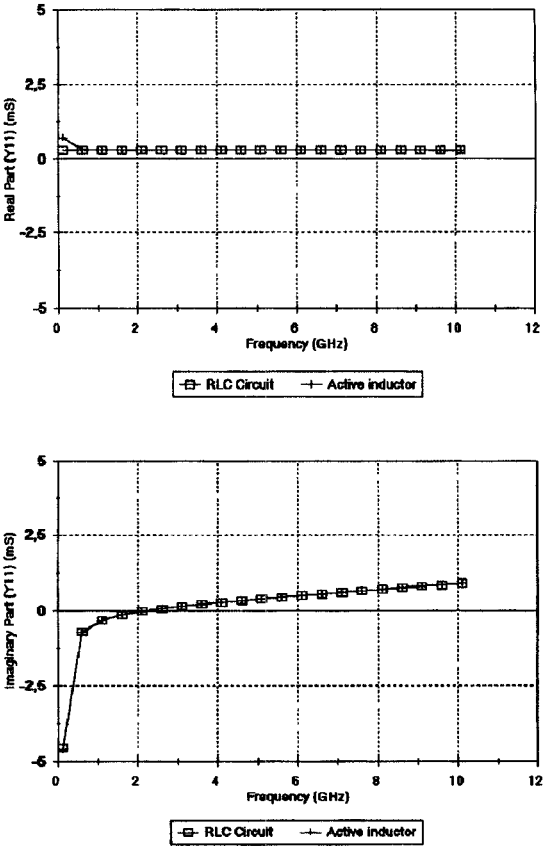


Fig. 22. Comparison of the admittance of the active inductive circuit shown in Fig. 20(a) with that of the ideal inductive circuit RLC where $L = 340\,\text{nH}, R = 3.5\,\text{k}\Omega, C = 0.016\,\text{pF}$.

Tables I and II display the influence of resistor R and capacitance C on the values of L_m, C_m, and $G_m\,(= 1/R_m)$ of the equivalent parallel circuit before the addition of bias circuitry. In the most cases, the devices biasing has not had a high impact on these results. Each FET is replaced by its complete model and the quality factor (Q) is computed at the 2 GHz. The values of the inductive circuits, Figs. 20(c), 20(d), 21(a), 21(c), 21(d), and 21(f), show that there exists intermediate values for (R) and (C) which $1/Q = 0$. We can obtain the same results $(1/Q = 0)$ for the other circuits, if (R) is upper than $3\,\text{k}\Omega$ or $C > 0.448\,\text{pF}$.

Curves of Figs. 22 and 23 display variations of the real and imaginary parts of the inductor, Figs. 20(a) and 21(a), respectively, as functions of the frequency when $R = 3\,\text{k}\Omega$ and $C = 0.448\,\text{pF}$. We compared these variations with the corresponding ones of parallel RLC circuit having $R = 3.5\,\text{k}\Omega, L = 340\,\text{nH}$ and $C = 0.16\,\text{pF}$ for the circuit shown in Fig. 20(a); $R = 5\,\text{k}\Omega, L = -350\,\text{nH}$ and $C = 0.16\,\text{pF}$ for Fig. 21(a). This curves prove than the representation of the inductive circuit by a parallel RLC circuit is appropriate.

C. Large Loss Inductors

Our study shows that adding up a resistor in the feedback loop of the large loss inductors greatly improves their quality factor although losses stay definitely more important compared to the losses in the previous circuits.

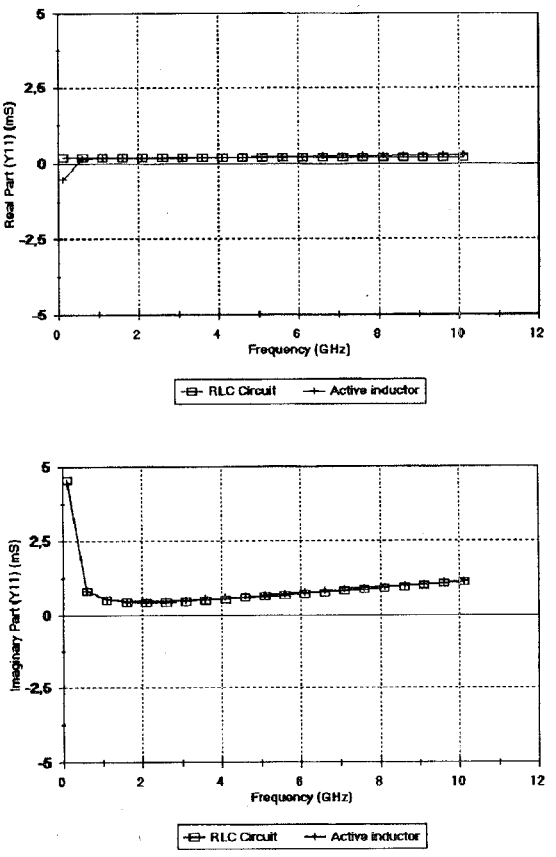


Fig. 23. Comparison of the admittance of the active inductive circuit [Fig. 21(a)] with that of the ideal inductive circuit RLC where $R = 5\,\mathrm{k}\Omega, L = -350\,\mathrm{nH}$ and $C = 0.016\,\mathrm{pF}$.

V. Conclusion

We have proposed an original method for the determination of all possible inductive circuits as a function of the number of FET's used, and improving the quality factor. The higher values obtained for the inductor, opens the door to direct application in the field of microwave, synthesis methods, well known and well mastered by the designers in the low frequency field. The excellent results enable the application of these structures particularly in active MMIC filters and oscillators.

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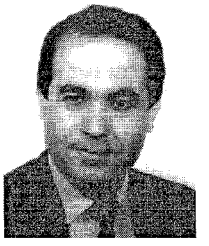

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